Course Title	**Computer Organization & Assembly Language Lab**
Course Code	**DC-221L**
Credit Hours	1
Category	Domain Core
Prerequisite	None
Co-Requisite	None
Follow Up	None
Course Description	Student should be able to • Understand the link between High-Level Language (C Language), Assembly Language (MIPS Assembly) and Machine Language. • Use the MIPS Assembly Language as an example. • The arithmetic of the computer. • The design of a basic 5-stage single cycle Processor. The design of a basic 5-stage pipelined Processor. • Data and Control hazards in pipelining. • Memory hierarchy Design. • Storage and I / O. • Designing and implementing a comprehensive hardware project. Instruction set architecture. Accumulator based, Stack Based and General Purpose Register Organization. Processor's Data Path. Design of a basic computer highlighting the timing and control system in instruction execution cycle. Interrupts, traps and signals. Comparison of Intel 80x86 and MIPS architectures. Addressing Modes. Mapping of High level language to corresponding assembly and machine language. Memory and Cache organization techniques. I/O techniques (Memory mapped and isolated I/O). Latest trends in Architectures.
Text Book(s)	Kip R. Irvine, Assembly Language for Intel Based Computers, Third Edition, 1999, Prentice-Hall Publishing, 1999, ISBN-10: 0132383101
Reference Material	Assembly Language Reference by Que. Corporation